In the Specification

Please amend the paragraph beginning at page 14, line 9 as follows:

One aspect of the present invention is a multiprocessor computer system 700 (such as the systems shown in Figures 7 and 8) comprising a plurality of processors 702, at least one main memory 704, at least one communication device 706, a plurality of caches 708, and a protection bit 712. The protection bit 712 is shown in Figures 9 and 10. In this embodiment, the plurality of processors 702 each have prefetcher logic and are capable of speculative execution. The at least one communication device 706 couples the plurality of processors 702 to the at least one main memory 704. The communication device 706 may be an interconnection network 706 (as shown in ~~Figure 9~~ Figure 7), a bus 706 (as shown in Figure 8), or any other communication device.